KLE Technological University | Creating Value, Leveraging Knowledge

Curriculum Structure and Curriculum Content for the Academic Batch – 2021-23
School /Department: Electronics & Communication Engineering
Program: Postgraduate

KLE Technological University | Creating Value, Leveraging Knowledge

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Vision and Mission

Vision

KLE Tech-School of Electronics and Communication (VLSI Design & Embedded System) will be well recognized nationally and internationally for excellence in its educational programs, pioneering research and impact on the industry and society.

Mission

1. To create a unique learning environment through rigorous curriculum of theory and practice that develops students' technical, scientific and professional skills, and qualities to succeed in wide range of electronics and computing businesses and occupations.
2. To nurture spirit of innovation and state-of-the-art research to advance the boundaries of disciplinary and interdisciplinary knowledge and its applications.
3. To collaborate within and beyond the discipline to create solutions that benefit humanity and society.

Program Educational Objectives (PEO's)

1. Graduates will demonstrate peer- recognized technical competency to solve contemporary problems in the analysis, design and development of electronic devices and systems.
2. Graduates will demonstrate leadership and initiative to advance professional and organizational goals with commitment to ethical standards of profession, teamwork and respect for diverse cultural background.
3. Graduates will be engaged in ongoing learning and professional development through pursuing higher education, and self-study.
4. Graduates will be committed to creative practice of engineering and other professions in a responsible manner contributing to the socio-economic development of the society.

Program Outcomes (PO's)

The graduates will have,

1. An ability to independently carry out research /investigation and development work to solve practical problems.
2. An ability to write and present a substantial technical report/document.
3. Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
4. An ability to use modern computational tools in modeling, simulation and analysis pertaining to VLSI Design and Embedded Systems.
5. An ability to work with integrity and ethics in their professional practice, having an understanding of responsibility towards society with sustainable development for lifetime.

Curriculum Structure-Overall

Semester	Total Program Credits: 88			
Course with course code	**I**	**II**	**III**	**IV**
	Data Structures using C 18EVEC701 (0-0-3)	Mathematical Thinking and Logical Reasoning 15EHSC701 (3-0-0)	Internship/ Mini Project 17EVEI801 (0-0-8)	Project Phase II / Major Project 17EVEW 802 (0-0-20)
	Analog Circuits 20EVEC702 (3-0-0)	Automotive Electronics and Communication 19EVEC701 (3-0-1)		
	CMOS VLSI Design 22EVEC704 (4-0-1)	Real Time Embedded Systems 19EVEC702 (3-0-1)	Project Phase I / Minor project 17EVEW801 (0-0-10)	
	Advanced Digital Logic Design 17EVEC710 (0-0-2)	Advanced Digital Logic Verification 19EVEC703 (0-0-3)		
	Machine Learning 22EVEC708 (2-0-1)	Analog & Mixed Mode VLSI Circuits 21EVEC704 (3-0-0)		
	RISC Architectures and Programming 17EVEC705 (4-0-1)	**Elective : 1** • Image & Video Processing(17EVEE701) (2-0-1) • MEMS(19EVEE701) (2-0-1) • System on Chip(19EVEE702) (2-0-1) • ASIC Design(19EVEE703) (2-0-1) • Testing & IC Characterization(19EVEE704) (2-0-1) **Elective : 2** • Standard Cell Design & Layout(17EVEE703) (2-0-1) • Low Power VLSI Circuits (19EVEE705) (2-0-1) • Internet of Things (19EVEE706) (2-0-1) • AUTOSAR(20EVEE707) (2-0-1) **Mini Project** 19EVEW701 (0-0-3)		
	Electronic System Design 17EVEC707 (0-0-3)			
Credits	**24**	**26**	**18**	**20**

Semester: I Semester M.Tech.

	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration
1.	18EVEC701	Data Structures using C	Core 1	0-0-3	3	6	80	20	100	2 hours
2.	20EVEC702	Analog Circuits	Core 2	3-0-0	3	4	50	50	100	3 hours
3.	17EVEC704	CMOS VLSI Design	Core 3	4-0-1	5	6	50	50	100	3 hours
4.	17EVEC710	Advanced Digital Logic Design	Core 4	0-0-2	2	4	100	00	100	3 hours
5.	18EVEC708	Machine Learning	Core 5	2-0-1	3	4	50	50	100	3 hours
6.	17EVEC705	RISC Architectures and Programming	Core 6	4-0-1	5	6	50	50	100	3 hours
7.	17EVEC707	Electronic System Design	Core 7	0-0-3	3	6	100	00	100	3 hours
TOTAL				**12-0-12**	**24**	**36**	**480**	**220**	**700**	

ISA: Continuous Internal Evaluation**ESA**: Semester End Examination **L**: Lecture **T**: Tutorials **P**: Practical

Semester: II Semester M.Tech.

	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration
1.	15EHSC701	Mathematical Thinking and Logical Reasoning	Core 8	3-0-0	3	3	50	50	100	3 hours
2.	19EVEC701	Automotive Electronics and Communication	Core 9	3-0-1	4	5	50	50	100	3 hours
3.	19EVEC702	Real Time Embedded Systems	Core 10	3-0-1	4	5	50	50	100	3 hours
4.	19EVEC703	Advanced Digital Logic Verification	Core 11	0-0-3	3	6	100	00	100	3 hours
5.	21EVEC704	Analog & Mixed Mode VLSI Circuits	Core 12	3-0-0	3	3	50	50	100	3 hours
6.	17EVEE701	Image & Video Processing	Elective 1	2-0-1	3	4	50	50	100	3 hours
	19EVEE701	MEMS								
	19EVEE702	System on Chip								
	19EVEE703	ASIC Design								
	19EVEE704	Testing & IC Characterization								
7.	17EVEE703	Standard Cell Design & Layout	Elective 2	2-0-1	3	4	50	50	100	3 hours
	19EVEE705	Low Power VLSI Circuits								
	19EVEE706	Internet of Things								
	20EVEE707	AUTOSAR								
8.	19EVEW701	Mini Project	Core 13	0-0-3	**3**	6	50	50	100	3 hours
TOTAL				**16-0-10**	**26**	**36**	**450**	**350**	**800**	

ISA: Continuous Internal Evaluation**ESA**: Semester End Examination **L**: Lecture **T**: Tutorials **P**: Practical

Semester: III Semester M.Tech.

	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration
1.	17EVEI801	Internship/ Mini Project	Core 14	0-0-8	8	16	50	50	100	3 hours
2.	17EVEW801	Project Phase I / Minor project	Core 15	0-0-10	10	20	50	50	100	3 hours
TOTAL				**0-0-18**	**18**	**36**	**100**	**100**	**200**	

ISA: Continuous Internal Evaluation**ESA**: Semester End Examination **L**: Lecture **T**: Tutorials **P**: Practical

Semester: IV Semester M.Tech.

	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration
1	17EVEW 802	Project Phase II / Major Project	Core 16	0-0-20	20	40	50	100	150	3 hours
TOTAL				**0-0-20**	**20**	**40**	**50**	**100**	**150**	

ISA: Continuous Internal Evaluation**ESA**: Semester End Examination **L**: Lecture **T**: Tutorials **P**: Practical

Semester: I Semester M.Tech.

Program: VLSI Design & Embedded Systems			
Course Title: Data Structures using C		**Course Code: 18EVEC701**	
L-T-P: 0-0-3	**Credits: 3**	**Contact Hours: 6**	
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**	
Teaching Hours: 25	**Examination Duration: 3 hrs**		

Chapter 01:C language features Pointers revisited, Strings, Structures – Basics, Structures and functions, Arrays of structures, Pointers to structures, Self Referential Structures, Unions and bit fields, Files.	5 Hrs
Chapter 02:Stacks and Queues Definition, Representation and Applications of stack. Definitions, representation and applications of linear, circular, queues, multiple queues, priority queue. Recursion	5 Hrs
Chapter 03:Lists Linked lists, singly, doubly, circular lists, definitions, representations. Implementation of list operations, applications – polynomial addition, addition of long integers. Linked stacks, Linked Queues	5 Hrs
Chapter 04:Trees Binary trees – Definitions, traversals (recursive and iterative versions), Building and searching, Threaded Binary trees, Trees and their applications	5 Hrs
Exchange sorts, Selection and tree sorts, Merge and radix sorts	5 Hrs
Text Book 1. Aaron M. Tenenbaum, et al, Data Structures using C, II Edition, PHI, 2006 2. Horowitz, Sahani, Anderson-Feed, Fundamentals of Data Structures in C, II Edition, University, 2008 **References** 1. E Balaguruswamy, The ANSI C programming Language, II Edition, PHI, 2010 2. Yashavant Kanetkar, Data Structures through C, II Edition, BPB public, 2010 3. Richard F. Gilberg, Behrouz A. Forouzan , Data Structures: A Pseudocode Approach With C, II Edition, Course Tec, 2009	
Lab: **1.** Programs on Pointer concepts. **2.** Programs on string handling functions, structures union And bit-files. **3.** Programming on files **4.** Programming on stacks data structures **5.** Programs on implementation of different queue data structures. **6.** Programs on implementation of different types of Linked lists **7.** Programs on Implementation of trees **8.** Programs to implement different sorting techniques. **9.** Programming on graph **10.** Programming on hashing tables **11.** Design and implement stack queue data structures **12.** Design and implement linked list data structures **13.** Project	

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Program: Digital Electronics			
Course Title: Analog Circuits		**Course Code: 20EVEC702**	
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 4**	
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**	
Teaching Hours: 40	**Examination Duration: 3 hrs**		

Content	Hrs
Chapter No. 1: Network Theorems Review of circuit analysis basics: KCL, KVL, Mesh and Nodal analysis. Circuit Analysis Techniques: Linearity and Superposition, Source Transformations, Thevenin's and Norton's Equivalent Circuits, Maximum Power Transfer, Delta-Wye conversion.	6 hrs
Chapter No. 2: First and Second Order circuits Order of a system, Concept of Time constant, System Governing equation, System Characteristic equation, Initial conditions, Transfer Functions (Fourier and Laplace domain representation)Frequency and Time response of RLC circuits	4 hrs
Chapter No. 3: Two Port Networks Admittance, Impedance and Hybrid Parameters. Transmission Parameters.	4 hrs
Chapter No. 4: Basic MOS DevicePhysics MOS Structure. Structure & Operation of MOS Transistor (MOSFET).The MOS System under external Bias MOSFET Current Voltage Characteristics. MOSFET Scaling and Small Geometry Effects. MOSFET Capacitances	4 hrs
Chapter No. 5: CMOS Amplifiers Biasing of MOS Stages, Realization of Current Sources, Common−Source Stage, Common−Gate Stage, Source Follower, Cascode Stage and Folded Cascode Amplifiers	5 hrs
Chapter No. 6: Current Mirrors Current Mirror circuits and Modeling. Figures of merit (output impedance, voltage swing). Widlar, Cascode and Wilson current Mirrors. Current source and Current sink.	5 hrs
Chapter No. 7: Basic Differential Amplifier Analysis Basic differential amplifier, Common mode and difference mode gain, CMRR, 5-pack and 7-pack Differential Amplifier, Performance parameters	6 hrs
Chapter No. 8: Design of 5pack and 7-pack differential amplifier, Stability and Frequency Compensation, Millers Compensation.	6 hrs

Reference Books:

1. A.S. Sedra & K.C. Smith, Microelectronic Circuits, 5th Edition, Oxford Univ. Press, 1999
2. Jacob Millman and Christos Halkias, Integrated Electronics, McGraw Hill,
3. John M Yarbrough, Digital Logic Applications and Design, Thomson Learning, 2001
4. David A. Bell, Electronic Devices and Circuits, 4th edition, PHI publication, 2007
5. Grey, Hurst, Lewis and Meyer, Analysis and design of analog integrated circuits, 4th edition.
6. Charles H Roth, Jr; Fundamentals of Logic Design, Thomson Learning, 2004.
7. Zvi Kohavi, Switching and Finite Automata Theory, 2ed, TMH
8. Ogata, Modern Control Theory, 4th ed, PHI.

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Program: VLSI Design & Embedded Systems			Teaching Hours
Course Title: CMOS VLSI Design		Course Code: 17EVEC704	
L-T-P: 4-0-1	Credits: 5	Contact Hours: 6 Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 72 Hrs	Examination Duration: 3 hrs		

Chapter No. 1. Introduction to VLSI and IC fabrication technology VLSI Design Flow, MOS theory, Introduction, nMOS / pMOS enhancement transistors, Comparison of BJTs and MOSFETs, Threshold voltage equation, MOS device design equations, MOS capacitance models, Second order effects: Sub-threshold conduction, Velocity Saturation and Mobility Degradation, Channel length modulation, Body Effect, Junction Leakage, Tunneling, Temperature Dependence. FinFET device, The root cause of short channel effects in twenty-first century MOSFETS, The thin body MOSFET concept, The FinFET and a new scaling path for MOSFETs, Ultra thin body FET.	10 hrs
Chapter No. 2 IC fabrication technology Semiconductor Technology - An Overview, Czochralski method of growing Silicon,Wafer cleaning process, Introduction to Unit Processes (Oxidation, Diffusion, Deposition, Ion-implantation), Basic CMOS technology - Silicon gate process, n-Well process, p-Well process, Twin-tub Process.	12 hrs
Chapter No. 3. DC Analysis of CMOS logic gates DC transfer characteristics of CMOS inverter, Beta Ratio Effects, Noise Margin, MOS capacitance models.	04 hrs
Chapter No. 4. Transient Analysis of CMOS logic gates Transient Analysis of CMOS Inverter, NAND, NOR and Complex Logic Gates, Gate Design for Transient Performance, Switch-level RC Delay Models, Delay Estimation, Elmore Delay Model, Power Dissipation of CMOS Inverter, Transmission Gates & Pass Transistors, Tristate Inverter.	06 hrs
Chapter No. 5. Designing High-Speed CMOS Logic Networks Stick Diagrams, Euler Path, Layout design rules, DRC, Circuit extraction, Latch up – Triggering Prevention, Gate Delays, Driving Large Capacitive Loads, Delay Minimization in an Inverter Cascade, Logical effort, BiCMOS Drivers.	10 hrs
Chapter No. 6. Combinational CMOS Circuit Design Pseudo nMOS, Clocked CMOS, Dynamic CMOS Logic Circuits, Dual-rail Logic Networks: CVSL, CPL.	05 hrs
Chapter No. 7. Sequential CMOS Circuit Design Sequencing static circuits, Circuit design of latches and flip-flops, Clocking- clock generation, clock distribution.	05 hrs

Text Books

1. John P. Uyemura, Introduction to VLSI Circuits and Systems, 1, Wiley, 2007
2. Neil Weste, David Harris & Ayan Banerjee, CMOS VLSI Design, 3, Pearson Ed, 2005
3. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 3, Tata McGraw, 2007
4. Sorab K. Ghandhi, VLSI Fabrication Principles, Wiley, 2nd edition, 1994

References

1. FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard
   By Yogesh Singh Chauhan, Darsen Duane Lu, Vanugopalan Sriramkumar, Sourabh Khandelwal, Juan Pablo Duarte, Navid Payvadosi, Ai Niknejad, Chenming Hu, Elsevier Publication, 2015
2. Wayne, Wolf, Modern VLSI design: System on Silicon, 3, Pearson Ed, 2005
3. Douglas A Pucknell and Kamran Eshraghian, Basic VLSI Design, 3, PHI, 2005

4. Phillip. E. Allen, Douglas R. Holberg, CMOS Analog circuit Design, 1, Oxford Uni, 2002

Lab:

1. Introduction to Cadence EDA tool.
2. Static and Dynamic Characteristic of CMOS inverter.
3. Layout of CMOS Inverter (DRC,LVS)
4. Static and Dynamic Characteristic of CMOS NAND2 and NOR2
5. Layout of NAND2, NOR2, XOR2 gates (DRC, LVS).
6. Design a Phase Detector using D-FF
7. Design complex combinational circuits and analyze the performance using Cadence tool.

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Program: VLSI Design & Embedded Systems			Teaching Hours
Course Title: Advanced Digital Logic Design		Course Code: 17EVEC710	
L-T-P: 0-0-2	Credits: 2	Contact Hours: 4 Hrs/week	
ISA Marks: 100	ESA Marks: -	Total Marks: 100	
Teaching Hours: 45 Hrs	Examination Duration: -		

Chapter No. 1. Digital Integrated Circuits Moore's law, Technology Scaling, Die size growth, Frequency, Power dissipation, Challenges in digital design, Design metrics, Cost of Integrated circuits, ASIC , Evolution of SoC ASIC Flow Vs SoC Flow, SoC Design Challenges. Introduction to CMOS Technology, PMOS & NMOS Operation, CMOS Operation principles, Characteristic curves of CMOS, CMOS Inverter and characteristic curves, Delays in inverters, Buffer Design, Power dissipation in CMOS, CMOS Logic, Stick diagrams and Layout diagrams. Setup time, Hold Time, Timing Concepts.	10 hrs
Chapter No. 2. Digital Building Blocks Basic Gates, Universal Gates, nand & nor Implementations. Decoder, encoder, code converters, Priority encoder, multiplexer, demultiplexer, Comparators, Parity check schemes, Multiplexer, De-multiplexer, Pass Transistor Logic, application of multiplexer as a multi-purpose logical element. Asynchronous and synchronous up-down counters, Shift registers. FSM Design, Mealy and Moore Modelling, Adder & Multiplier concepts, Memory Concept	10 hrs
Chapter No. 3. Logic Design Using Verilog Evolution & importance of HDL, Introduction to Verilog, Levels of Abstraction, Typical Design Flow, Lexical Conventions, Data Types Modules, Nets, Values, Data Types, Comments, arrays in Verilog, Expressions, Operators, Operands, Arrays, memories, Strings , Delays , parameterized designs Procedural blocks, Blocking and Non-Blocking Assignment, looping, flow Control, Task, Function, Synchronization, Event Simulation. Need for Verification, Basic test bench generation and Simulation	12 hrs
Chapter No. 4. Principles of RTL Design Verilog Coding Concepts, Verilog coding guide lines: Combinational, Sequential, FSM. General Guidelines, Synthesizable Verilog Constructs, Sensitivity List, Verilog Events, RTL Design Challenges, Clock Domain Crossing. Verilog modelling of combinational logic and sequential logic	8 hrs
Chapter No. 5. Design and simulation of Architectural building blocks Basic Building blocks design using Verilog HDL: Arithmetic Components – Adder, Subtractor, and Multiplier design, Data Integrity – Parity Generation circuits, Control logic – Arbitration, FSM Design – overlapping and non-overlapping Mealy and Moore state machine design	10 hrs

Reference Books:

1. Digital Design by Morris Mano M, 4th Edition.
2. Verilog HDL: A Guide to Digital Design and Synthesis by Samir Palnitkar, 2nd Edition
3. Principles of VLSI RTL Design: A Practical Guide by Sapan Garg, 2011 Tools: 1. NC Verilog, NC Sim, CVER + GTKWave, VCSMX, Modelsim for Verilog 2. Microwind for layout.

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Program: Digital Electronics	Teaching

Course Title: Machine learning		Course Code: 18EVEC708	Hours
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 40 Hrs	Examination Duration: 3 hrs		

Chapter No. 1: Introduction Introduction What is Machine Learning? Applications of Machine Learning, Types of Machine Learning: Supervised, Unsupervised and Reinforcement learning, Dataset formats, Basic terminologies.	**05 Hrs**
Chapter No. 2: Supervised Learning Linear Regression, Logistic Regression Linear Regression: Single and Multiple variables, Sum of squares error function, The Gradient descent algorithm, Application, Logistic Regression, The cost function, Classification using logistic regression, one-vs-all classification using logistic regression, Regularization.	**10 Hrs**
Chapter No. 3: Supervised Learning: Neural Network Introduction to perception learning, Implementing simple gates XOR, AND, OR using neural network. Model representation, Gradient checking, Back propagation algorithm, Multi-class classification, Application-classifying digits, SVM.	**10 Hrs**
Chapter No. 4: Unsupervised Learning: Clustering Introduction, K means Clustering, Algorithm, Cost function, Application.	**05Hrs**
Chapter No. 5: Unsupervised Learning: Dimensionality reduction Dimensionality reduction, PCA- Principal Component Analysis. Applications, Clustering data and PCA.	**05Hrs**
Chapter No. 6: Machine Learning System Design Evaluating a hypothesis, Model selection, Bias and variance, error analysis, error metrics for skewed classes. Building a Model.	**05 Hrs**

Text Book (List of books as mentioned in the approved syllabus)

1. Tom Mitchell, Machine Learning, 1, McGraw-Hill. , 1997
2. Christopher Bishop, Pattern Recognition and Machine Learning, 1, Springer, 2007

References

1. Video lectures by : Andrew Ng, Co-founder, Coursera; Adjunct Professor, Stanford University; formerly head of Baidu AI Group/Google Brain https://www.coursera.org/learn/machine-learning#
2. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning : Data Mining, Inference and Prediction, 2, Springer, 2009

Implementation Assignments:

1. Assignments are designed to explore the concepts like
   - Supervise and unsupervised learning,
   - Clustering,
   - Regression and estimation
2. Motivate students to take up open challenges like Kaggle, walmart, ect
3. To explore different Machine Learning Tools/ Libraries.

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Program: VLSI Design & Embedded Systems			Teaching Hours
Course Title: RISC Architectures and Programming		Course Code: 17EVEC705	
L-T-P: 4-0-1	Credits: 5	Contact Hours: 6 Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50 Hrs	Examination Duration: 3 hrs		
1. The 32-bit RISC Architecture: The Acorn RISC machine, Architectural inheritance, Architecture of ARM7TDMI, ARM programmers' model, ARM development tools, 3 stage pipeline ARM organization, ARM instruction execution.			**06 Hrs**
2. Instruction sets, Assembly and Embedded C Programming: Features of ARM Instruction, Data processing instruction, Branch/Control instruction and Data Transfer/Load store instruction. Software interrupt instruction, Program status register instruction, Conditional execution, Example programs, 16bit Instruction set-The Thumb programmer model, ARM-Thumb interworking, Thumb branch instructions, Data processing instructions, Single/Multiple register load store instruction, Stack operation, Software interrupt instructions, example programs.			**06 Hrs**
3. Introduction to LPC2148 and Embedded C programming: Architectural Overview of LPC2148, Features and Memory mapping of LPC2148, Interfacing of Basics peripherals to LPC2148 and programming using Embedded C.			**04 Hrs**
4. Exception Handling: Introduction, Interrupts, error conditions, processor exception sequence, the vector table, Exception handlers, Exception priorities, Procedures for handling exceptions.			**04 Hrs**
5. Memory Hierarchy Design: Cache basics, Miss rate and penalty, Cache Hierarchy, Memory Organizations, Memory Hierarchy.			**06 Hrs**
6. Pipelining: Linear pipeline processor, Nonlinear pipeline processor, Instruction pipeline design, Branch handling techniques, Arithmetic pipeline design, Computer arithmetic principles, Static arithmetic pipeline, Multifunctional arithmetic pipeline.			**08 Hrs**
7. Cortex M4: Functional description, programmer's model, memory protection unit, nested vectored interrupt controller.			**06 Hrs**
8. Multi-Core Architectures: Introduction to Intel Architecture, How an Intel Architecture System works, Basic Components of the Intel Core 2 Duo Processor: The CPU, Memory Controller, I/O Controller.			**07 Hrs**
9. Current Trends in Intel Architectures and Applications: Seminar on current trends in Intel Architectures			**03 Hrs**

Text Books

1. "ARM System- on-Chip Architecture" by 'Steve Furber', LPE, Second Edition.
2. "ARM Assembly Language fundamentals and Techniques" by William Hohl, CRC press, 2009.
3. D. A. Patterson and J. L. Hennessey "Computer Organization and Design", Morgan, Kaufmann,2002
4. H. Jonathan Chao and Bin Liu, "High performance switches & routers", Wiley Interscience, 2007.
5. Kai Hwang, "Advanced Computer Architecture – TMH – 1993
6. Web resources for Example Architectures of INTEL and Texas Instruments: http:/ /download.intel.com/design/intarch/papers/321087.pdf

References

1. Kai Hwang, Faye A. Briggs, Computers Architecture and Parallel Processing – MGH – 1985
2. David E Culler, Jaswinder Pal Singh, Anoop Gupta "Parallel Computer Architecture", Harcourt Asia Pte Ltd 2000
3. Stalling W." Computer Organization and Architecture- Designing for performance" PHI,2005
4. D. Sima,T. Fountain, P.Kasuk," Advanced Computer Architecture-A Design Space Approach" Addisson Wesley,1997.
5. M. J. Flynn,"Computer Architecture, Pipelined And Parallel Processing", Narosa Publications, 1998.

List of Experiments:

1. Write an ALP to verify data transfer w.r.t memory to achieve following,
    i. 8-bit data transfer and exchange
    ii. 16-bit data transfer and exchange
    iii. 32-bit data transfer and exchange
2. Write an ALP for Tables and lists to do following,
    i. Add an entry to a list
    ii. Remove an element from the queue
3. Write an ALP to pass parameters to a subroutine,
    i. Ascending order
    ii. Descending order
4. Write an ALP for following,
    i. Finding length of a string
    ii. Compare two strings for equality
    iii. To find whether given string is palindrome
5. Write a 'C' program & demonstrate an interfacing of Alphanumeric LCD 2X16 panel to LPC2148Microcontroller
6. Write a 'C' program & demonstrate an interfacing of Seven segment to LPC2148 Microcontroller.
7. Write a 'C' program & demonstrate an interfacing of UART to LPC2148 Microcontroller.
8. Write a 'C' program & demonstrate an interfacing of ADC to LPC2148 Microcontroller.
9. Write a 'C' program & demonstrate an interfacing of Keypad to LPC2148
10. Write a 'C' program & demonstrate interface DAC to LPC2148
11. Develop a code for electronic voting machine.

Reference Books

1. "ARM System- on-Chip Architecture" by 'Steve Furber", LPE, Second Edition.
2. "Embedded Systems- Architecture, Programming and Design" by Raj Kamal, TMH
3. Dr. K.V.K.K. Prasad, "Embedded/Real-time systems: concepts, Design & Programming", published by dreamtech press.

Manual

1. LPC2148 datasheet by NXP.

2. LPC2148 board manual by ALS, Bangalore.

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Program: VLSI Design & Embedded Systems			
Course Title: Electronic System Design		Course Title: 17EVEC707	
L-T-P: 0-0-3	Credits: 3	Contact Hours:6 Hrs/week	
ISA Marks: 100	ESA Marks:	Total Marks: 100	
Teaching Hours: 25 Hrs	Examination Duration: --		
To level specifications, Block level specifications, Timing of micro architecture, Verification and test plan, Schematic capture			05 Hrs
Simulation, Advanced simulation, Signal Integrity			05 Hrs
PCB layout- Floor planning, component pre planning, PCB printing- 2 layer			05 Hrs
Functionality and performance check, Failure analysis, Validation and system integration			05 Hrs
System Analysis			05 Hrs

References

1. A. S Sedra and KC Smith, Microelectronic circuits, Oxford, 1998.
2. G.L. Ginsberg, Printed Circuit Design, McGraw Hill, 1991.

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Program: VLSI Design & Embedded Systems		
Course Title: Mathematical Thinking and Logical Reasoning		**Course Code:** 15EHSC701
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 40	**Examination Duration: 3 hours**	

1. Quantitative Aptitude	10 hrs
2. Analytical Puzzles	4 hrs
3. Syllogistic Logic	3 hrs
4. Verbal Reasoning	9 hrs
5. Visual Reasoning	6 hrs
6. Advanced Lateral Thinking	8 hrs

Text Books

1. A Modern Approach to Verbal and Non – Verbal Reasoning – R. S. Aggarwal, Sultan Chand and Sons, New Delhi.
2. Quantitative Aptitude – R. S. Aggarwal, Sultan Chand and Sons, New Delhi

Reference Books:

1. Verbal and Non – Verbal Reasoning – Dr. Ravi Chopra, MacMillan India
2. Lateral Thinking – Dr. Edward De Bono, Penguin Books, New Delhi

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Program: VLSI Design & Embedded Systems			
Course Title: Automotive Electronics and Communication		Course Code: 19EVEC701	
L-T-P: 3-0-1	Credits: 4	Contact Hours: 5 hrs	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50	Examination Duration: 3 hrs		

Chapter No: 1.Automotive Systems, Design cycle and Automotive industry overview Overview of Automotive industry, Vehicle functional domains and their requirements, automotive supply chain, global challenges. Role of technology in Automotive Electronics and interdisciplinary design. Introduction to modern automotive systems and need for electronics in automobiles and application areas of electronic systems in modern automobiles, Introduction to power train, Automotive transmissions system ,Vehicle braking fundamentals, Steering Control, ,Overview of Hybrid Vehicles, ECU Design Cycle : Types of model development cycles(V and A) , Components of ECU, Examples of ECU on Chassis, Infotainment, Body Electronics and cluster.	9 hrs
Chapter No: 2. Embedded system in Automotive Applications & Automotive safety systems Automotive grade microcontrollers: Architectural attributes relevant to automotive applications, Automotive grade processors ex: Renesas, Quorivva, and Infineon. EMS: Engine control functions, Fuel control, Electronic systems in Engines , Development of control algorithm for EMS, Look-up tables and maps, Need of maps, Procedure to generate maps, Fuel maps/tables, Ignition maps/tables, Engine calibration, Torque table, Dynamometer testing Safety Systems in Automobiles: Active and Passive safety systems: ABS, TCS, ESP, Brake assist, Airbag systems etc.	10 hrs
Chapter No: 3. Automotive Sensors and Actuators Sensor characteristics, Sensor response, Sensor error, Redundancy of sensors in ECUs, Avoiding redundancy, Smart Nodes, Examples of sensors: Accelerometer (knock sensors),wheel speed sensors, Engine speed sensor, Vehicle speed sensor, Throttle position sensor, Temperature sensor, Mass air flow (MAF) rate sensor, Exhaust gas oxygen concentration sensor, Throttle plate angular position sensor, Crankshaft angular position/RPM sensor, Manifold Absolute Pressure (MAP) sensor. Actuators: Engine Control Actuators, Solenoid actuator, Exhaust Gas Recirculation Actuator.	9 hrs
Chapter No: 4. Automotive communication protocols Overview of Automotive communication protocols : need for communication in Automotive, overview of vehicle network architecture, need for CAN in Automotive, CAN Bus logic ,CAN frame formats, CAN bus fault confinement, LIN , Flex Ray, MOST.	10 hrs
Chapter No: 5. Advanced Driver Assistance Systems (ADAS) and Functional safety standards Advanced Driver Assistance Systems (ADAS):Examples of assistance applications: Lane Departure Warning, Collision Warning, Automatic Cruise Control, Pedestrian Protection, Headlights Control, Connected Cars technology and trends towards Autonomous vehicles. Functional Safety: Need for safety standard-ISO 26262, safety concept, safety process for product life cycle, safety by design, validation.	7 hrs
Chapter No: 6. Diagnostics Fundamentals of Diagnostics: Basic wiring system and Multiplex wiring system, Preliminary checks and adjustments, Self-diagnostic system. Fault finding and corrective measures, Electronic transmission checks and Diagnosis, Diagnostic procedures and sequence, On board and off board diagnostics in Automobiles, OBDII, Concept of DTCs, DLC, MIL, Freeze Frames, History memory, Diagnostic tools, Diagnostic protocols: KWP2000 and UDS.	5 hrs

Text books:

1. William B. Ribbens, Understanding Automotive Electronics, 6, Newnes Publications, 2003

2. Denton.T , Automobile Electrical and Electronic Systems, Edward Arnold , 1995

References:

1. William T.M , Automotive Electronic Systems, Heiemann Ltd., London , 1978
2. Nicholas Navet , Automotive Embedded System Handbook, CRC Press , 2009

Lab:

1. Demonstration of cut section modules: Engine, Transmission , Steering, Braking, Suspension - Automobile dept.
2. Electronic engine control system: Injection and Ignition control system Transmission trainer modules
3. Modeling an engine Vehicle model simulation with Simulink using PI CONTROLLER
4. Basic gate logic simulation and modeling using Simulink and realization on the hardware platform.
5. Seat belt warning system simulation and modeling using Simulink and realization on the hardware platform. Vehicle speed control based on the gear input simulation and modeling using Simulink and realization on the hardware platform.
6. Throttle control modeling and simulation using Simulink and realization on the hardware platform.
7. Accelerator pedal interfacing software modeling and simulation using Simulink and realization on the hardware platform.
8. Develop matlab code for stepper motor control and convert it to Simulink model and port it to embedded hardware

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Program: VLSI Design & Embedded Systems			
Course Title: Real Time Embedded System		Course Code: 19EVEC702	
L-T-P: 3-0-1	Credits: 4	Contact Hours: 5 Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 45 Hrs	Examination Duration: 3 hrs		

1. Building blocks: Real Time System, Types, Real Time Computing, Design Issue, Sample Systems, Hardware Requirements- Processor in a system, System Memories, System I/O, De-bouncing, Other Hardware Devices (A/D, D/A, USART, Watchdog Timers, Interrupt Controllers). Device Drivers, Interrupt Servicing Mechanism & Interrupt Latency.	**12 Hrs**
2. Advanced Processors: Automotive Grade Processors: AEC-Q100 qualification, Qorivva 32-bit Microcontrollers, MPC577XK for ADAS, AURIX from Infineon, Tricore Architecture, Renasas RL78/D1x (Automotive Only)	**10 Hrs**
3. Real Time Operating System: Interrupt driven systems, foreground/background systems, full featured rtos, POSIX, buffering data, mailboxes, critical regions, semaphores, event flags & signals, deadlock, process stack management, dynamic allocation.	**04 Hrs**
4. Case Studies: Mucos/ VX Works Functions – System level, task service, time delay, memory allocation, semaphore, mailbox, queue. Example systems: Coding for Automatic chocolate vending machine using MUCOS & Coding for sending application layer byte streams on a TCP/IP Network using Vx Works.	**06 Hrs**
5. Process of Embedded System Development: Development process, requirements engineering, design, implementation, integration & testing, packaging, configuration management, managing embedded system development, embedded system fiascos.	**08 Hrs**
6. Current trends, ethical & environmental issues The students shall give seminars on current trends in the field of RTES, ethical, & environmental issues.	**05 Hrs**

Text Books

1. Philip. A. Laplante, "Real-Time Systems Design and Analysis- an Engineer's Handbook"- Second Edition, PHI Publications.
2. Rajkamal, "Embedded Systems: Architecture, Programming and Design", Tata McGraw Hill, New Delhi, 2003.
3. Dr. K.V.K K Prasad, "Embedded Real Time Systems: Concepts Design and Programming", Dreamtech Press New Delhi, 2003.

References

1. Joseph Yiu, "The Definitive guide to ARM CORTEX –M3 & CORTEX-M4 Processors", Elsevier, Newnes, 2014.
2. Steve Furber "ARM System –on – Chip Architecture" Second Edition, Pearson Education
3. David E. Simon, "An Embedded software primer", Pearson Education, 1999..
4. David A. Evesham, "Developing real time systems – A practical introduction", Galgotia Publications, 1990
5. William Hohl, "ARM Assembly Language Fundamentals & Techniques", CRC Press
6. C. M. Krishna, "Real Time Systems" MGH, 1997
7. Jane W.S. Liu, "Real-Time Systems", Pearson Education Inc., 2000

Back to SEM II

Program: VLSI Design & Embedded Systems			
Course Title: Advanced Digital Logic Verification		Course Code: 19EVEC703	
L-T-P: 0-0-3	Credits: 3	Contact Hrs: 6 hrs/week	
ISA Marks: 100	ESA Marks: ---	Total Marks: 100	
Teaching Hrs: 50	Exam Duration: 3 hrs		

Chapter No. 1. Verification Concepts Concepts of verification, importance of verification, Stimulus vs Verification, functional verification, test bench generation, functional verification approaches, typical verification flow, stimulus generation, direct testing, Coverage: Code and Functional coverage, coverage plan.	10 hrs
Chapter No. 2. System Verilog – Language Constructs System Verilog constructs - Data types: two-state data, strings, arrays: queues, dynamic and associative arrays, Structs, enumerated types. Program blocks, module, interfaces, clocking blocks, modports.	10 hrs
Chapter No. 3. System Verilog – Classes & Randomization SV Classes: Language evolution, Classes and objects, Class Variables and Methods, Class instantiation, Inheritance, and encapsulation, Polymorphism. Randomization: Directed Vs Random Testing. Randomization: Constraint Driven Randomization.	12 hrs
Chapter No. 4. System Verilog – Assertions & Coverage Assertions: Introduction to Assertion based verification, Immediate and concurrent assertions. Coverage driven verification : Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.	8 hrs
Chapter No. 5. Building Testbench Layered testbench architecture. Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface	10 hrs
References: 1. System Verilog LRM 2. Chris Spear, Gregory J Tumbush - SystemVerilog for verification - a guide to learning the testbench language features - Springer, 2012 3. Step-by-Step Functional Verification with SystemVerilog and OVM by Sasan Iman SiMantis Inc. Santa Clara, CA Spring 2008 Tools: 1. NC Verilog, NC Sim, VCSMX for System.	

Back to SEM II

Program: VLSI Design & Embedded Systems			
Course Title: Analog and Mixed mode VLSI Circuits		Course Code: 21EVEC704	
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 40	Examination Duration: 3 hours		
Chapter 01: Basic Current reference, and Voltage (Bandgap) reference circuits, OPAMP based references, Current mode bandgap reference			06
Chapter 02: Bidirectional analog switch, Sample and Hold circuit, Basic Comparator architecture, non-idealities (offset error, bandwidth consideration), Dynamic comparator , Sense amplifier			03
Chapter 03: DAC architecture, Weighted Resistor and R-2R network, their Limitations, Current source based DAC			07
Chapter 04: ADC basics, Flash ADC, Tracking ADC , Dual slope ADC, SAR ADC, and their applications			10
Chapter 05: Pipeline ADC architecture,algorithm and Sigma-Delta ADC			06
Chapter 06: PLL-operating principles, Phase detector and VCO; Phase frequency Detector, Charge pump models, stability issues, Jitter in PLL.			08

Text Books

1. Phillip. E. Allen, Douglas R. Holberg, "CMOS Analog circuit Design" Oxford University Press, 2002.
2. Baker, Li, Boyce, "CMOS: Circuit Design, Layout and Simulation", Prentice Hall of India, 2000

Reference Books

1. N. Weste and K. Eshranghian, Principles of CMOS VLSI Design, Addison Wesley. 1985.
2. J. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall India, 1997
3. C. Mead and L. Conway, Introduction to VLSI Systems, Addison Wesley, 1979.
4. B Razavi 'Design of Analog CMOS Integrated Circuits' First Edition McGraw Hill 2001

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Program: VLSI Design & Embedded Systems			
Course Title: Image and Video Processing		Course Code: 17EVEE701	
L-T-P: 2-0-1	Credits: 3	Contact Hrs: 4 hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hrs: 40	Exam Duration: 03 hrs		

1	**Introduction**: 2D systems, Mathematical Preliminaries- FT, Z-transform, Optical and Modulation Transfer Functions (OTF and MTF). Matrix theory, Image perception: Light, Luminance, Brightness, Contrast, MTF of the visual system, Visibility function, Monochrome Vision Models, Fidelity criteria, Color Representation, Color Vision Models, Temporal Properties of Vision.	2 hrs
2	**Image sampling and Quantization:** 2D Sampling theory, Quantization, Optimal Quantizer, Compander and Visual Quantization.	2 hrs
3	**Image Transforms:** 2D orthogonal and unitary transforms, DFT, DCT, Harr, KLT	4hrs
4	**Image Enhancement**: Histograms Modeling, Spatial operations, Transform operations, Multispectral Image Enhancement,	4hrs
5	**Image Filtering and Restoration:** Image Observation Models, Inverse and Weiner filtering , Frequency Domain Filters. Smoothing Splines and Interpolation.	4hrs
6	**Basics of Video:** Analog Video, Digital Video	2 hrs
7	**Two dimensional motion estimation:** Optical flow methods**,** Block based methods, Bayesian methods**.**	7 hrs

Text books

1. Jain, A.K., Fundamentals of Digital Image Processing, 3rd Edision, Pearson Education (Asia) 2013
2. A. Murat Tekalp, Digital Video processing Pearson Education (Asia) Pte. Ltd.
3. Li and, Z. Drew, M.S. Fundamentals of Multimedia, Pearson Education (Asia) Pte. Ltd,. 2010.

References books

1. Gonzalez, Rafael C., Woods, Richard E. and Eddins Steven L., Digital Image Processing Using Matlab, Pearson Education (Asia) Pvt. Ltd.,
2. Al. Bovik, Essential guide to Video Processing, Academic Press

Implementation:

Implementation assignments are designed using opencv/c++ to explore the concepts like

1. Image enhancement techniques
2. Image transforms.
3. Image restoration technique
4. Develop an image processing application to assist
    a. ADAS

b. Agriculture
c. Defense
d. Health Care
e. Surveillance and Forensics
f. Remote sensing

5. Track an object in video
6. Optimal use of surveillance video

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Program: VLSI Design & Embedded Systems		
Course Title: MEMS		Course Code: 19EVEE701
L-T-P: 2-0-1	Credits: 3	Contact Hrs: 4
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40	Exam Duration: 3 hrs	

No	Content	Hrs
1	**Overview of MEMS and Microsystems** Evolution of Microsystems, Miniaturization, Applications, Working principles of Microsystems: Introduction to Micro-sensors, Micro-actuation, Example of MEMS with Micro-actuators – Airbag	5
2	**Micro-fabrication** Different structures used for MEMS devices (combination of Mechanical, electrical), How to create these structures	2
	Materials for MEMS and Microsystems: Silicon as a preferred material, Silicon compounds, GaAS, Quartz, Polymers, piezo-resistors; Machining processes (Bulk, Surface and LIGA processes). Unit processes in VLSI, Oxidation, Diffusion, Deposition, Etching, Photolithography	8
3	**Sensing Techniques and Examples:** PZR, PZE, and Capacitive sensing techniques, Modeling, Design and Analysis with example for each technique. Numerical problem for each technique.	10
4	**Case studies –** MEMS resonator, PZR accelerometer (Commercial)	5
5	**Scaling laws in miniaturization:** Introduction to scaling, scaling in geometry, electrostatic forces, EM forces, Electricity, Numerical problems.	4
6	**Modeling:** Modeling techniques: Mathematical modeling, Electrical modeling (Lumped modeling), Mechanical Modeling, MEMS CAD tools. MEMS as Inductor, Capacitor, Micro-Characterization.	6

Text Book:

*"*MEMS and Microsystems – Design and Manufacture*", Tai-Ran Hsu, TMH Edition*

References:

"*Micro system Design*", Stephen D. Senturia, Kluwer Academic Publishers, 2001.

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Program: VLSI Design & Testing			
Course Title: System on Chip		Course Code: 19EVEE702	
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4	
CIE Marks: 50	SEE Marks: 50	Total Marks: 100	
Teaching Hours: 50	Examination Duration: 3 hours		

1. **Verification and Technology Options:** Overview of verification, challenges in verification of SOC, Simulation technologies, Static technologies, Formal technologies, Physical verification and analysis, comparing verification options.	10 hrs
2. **Verification Methodology:** Verification plans, Testbench creation, Testbench migration, Verification languages, Verification device test, System level verification, Verification IP Reuse, Verification approaches.	10 hrs
3. System level Verification: System design, System verification, Applying the system level testbench, System testbench migration, Bluetooth SOC.	10 hrs
4. Static Netlist Verification: Netlist verification, Bluetooth SOC arbiter, Equivalence checking, Equivalence checking methodology, RTL to RTL verification, RTL to Gate level netlist verification, Gate level netlist to Gate level, Static timing verification and analysis**.**	10 hrs
5. SOC Testing: Importance of system on chip testing, SOC test issues, FPGA Testing: Overview of FPGA, Testing approaches, BIST of programmable resources, Embedded processor based testing**.**	10 hrs

Text Books

1. Prakash Rashinkar, Peter Paterson, Leena Singh, " SOC Verification –Methodology and Techniques", Springer 2000

2. Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, "System-on-chip Test Architectures", 2008.

Reference books

1. J-M. Berge, O. Levia, J. Rouillard: Hardware/Software Co-Design and Co-Verification, Kluwer, 1997.

2. M. L. Bushnell and V. D. Agrawal, Essential of Electronics Testing for Digital, Memory and Mixed-Signal Circuits, Kluwer Academic Publishers, 2001.

3. Thomas Kropf, "Introduction to Formal Hardware Verification", Springer 1999.

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Program: VLSI Design & Embedded Systems		
Course Title: ASIC Design		Course Code: 19EVEE703
L-T-P: 2-0-1	Credits: 3	Contact Hrs: 4
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 24	Exam Duration: 3 hrs	

Content	Hrs
Chapter No. 1. Introduction to ASIC ASIC types, design flow, economics of ASIC	4 hrs
Chapter No. 2. ASIC design library and Logic cell Transistor as register, transistor parasitic capacitance, Logic Effort, Data Path Elements, Adders, Multiplier, Sequential logic cells, I/O cell.	5 hrs
Chapter No. 3. Logic Synthesis and Simulation Logic synthesis, FSM synthesis, structural simulation, static timing analysis, delay models	5 hrs
Chapter No. 4. ASIC Construction Floor planning and placement and routing Physical Design, System Partitioning, Estimating ASIC size, partitioning methods.	5 hrs
Chapter No. 5. Floor planning and placement and routing Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.	5 hrs

Text Books:

1. M.J.S .Smith, - “Application - Specific Integrated Circuits” – Pearson Education, 2003.
2. Randall L Geiger, Phillip E. Allen, “Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits”, McGraw Hill International Company, 1990.

References:

1. Jose E.France, Yannis Tsividis, “Design of Analog-Digital VLSI Circuits for Telecommunication and signal processing”, Prentice Hall, 1994.
2. Andrew Brown, - “VLSI Circuits and Systems in Silicon”, McGraw Hill, 1991.
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, “Field Programmable Gate Arrays”- Kluwer Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, “Analog VLSI Signal and Information Processing “, McGraw Hill, 1994.
5. S. Y. Kung, H. J. Whilo House, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1985.

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Program: VLSI Design & Embedded Systems		
Course Title: Testing & IC Characterization		Course Code: 19EVEE704
L-T-P: 2-0-1	Credits: 3	Contact Hrs: 4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40	Exam Duration: 03 hrs	

Content	Hrs
Chapter No. 1. Verification Concepts Concepts of verification, importance of verification, Stimulus vs Verification, functional verification, test bench generation, functional verification approaches, typical verification flow, stimulus generation, direct testing, Coverage: Code and Functional coverage, coverage plan.	10 hrs
Chapter No. 2. System Verilog – Language Constructs System Verilog constructs - Data types: two-state data, strings, arrays: queues, dynamic and associative arrays, Structs, enumerated types. Program blocks, module, interfaces, clocking blocks, modports.	10 hrs
Chapter No. 3. System Verilog – Classes & Randomization SV Classes: Language evolution, Classes and objects, Class Variables and Methods, Class instantiation, Inheritance, and encapsulation, Polymorphism. Randomization: Directed Vs Random Testing. Randomization: Constraint Driven Randomization.	12 hrs
Chapter No. 4. System Verilog – Assertions & Coverage Assertions: Introduction to Assertion based verification, Immediate and concurrent assertions. Coverage driven verification : Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.	8 hrs
Chapter No. 5. Building Testbench Layered testbench architecture. Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface	10 hrs

References:

1. System Verilog LRM
2. Chris Spear, Gregory J Tumbush - SystemVerilog for verification - a guide to learning the testbench language features - Springer, 2012
3. Step-by-Step Functional Verification with SystemVerilog and OVM by Sasan Iman SiMantis Inc. Santa Clara, CA Spring 2008 Tools: 1. NC Verilog, NC Sim, VCSMX for System.

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Program: VLSI Design & Embedded Systems			
Course Title: Standard Cell Design and Layout	**Course Code: 17EVEE703**		
L-T-P: 2-0-1	**Credits: 3**	**Contact Hrs: 4**	
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**	
Teaching Hrs: 24		**Exam Duration: 3 hrs**	
Chapter No. 1. Introduction IC design flows. Use of standard cell elements vs. custom design and Gate array paradigms. Introduction to memory types and construction of memory elements.			8 hrs
Chapter No. 2. Standard cell library composition and usage Types of standard cell elements. Logical and functional elements, primitives and complex macros. Sequential elements and register files. (Flip flop and latch design). Data path elements. Library size vs. usage in standard flows. Drive strength and cell families. Layout of library elements – single height, double height cells. Power Management cells.			8 hrs
Chapter No. 3. Standard cell characterization Usage of standard cells by various tools. Information needed at each stage of design flow. Characterization parameters, setup and runs across PVT corners. Library representation formats. (Gate level simulation, synthesis, timing, layout, timing, LVS, DRC)			8 hrs
References: Standard cell and memory library documentation by Vendors 90nm EDK library			

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Program: VLSI Design & Embedded Systems			
Course Title: Low Power VLSI Circuits		Course Code: 19EVEE705	
L-T-P: 2-0-1	Credits: 3	Contact Hours:4	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 40	Examination Duration: 3 hours		

1: Introduction to low power VLSI design: Need for Low Power VLSI Chips, sources of power dissipation. Device and Technology impact on Low Power, dynamic power dissipation in CMOS. Power Estimation.	6Hrs
2: Power analysis: Simulation Power Analysis, Spice circuits simulator, gate level logic simulator, Probabilistic power analysis	5Hrs
3: A new CMOS driver model for transient analysis and power dissipation analysis, low power design of off-chip drivers and transmission lines: a branch and bound approach.	5Hrs
4: Different levels of power optimization Low Power Design; circuit Level, logic Level, Low Power Architecture.	7Hrs
5: Floor plan design with low power considerations, optimal drivers of high-speed low power ics, retiming sequential circuits for low power	5Hrs
6: Clock Distribution: Low Power Clock distribution, single driver versus distributed buffers. Power management: Power & performance management,switching activity reduction, parallel architecture.	4Hrs
7:Algorithmic level methodologies for power reduction: Algorithm and architectural level methodologies-algorithmic level analysis & optimization, architecture level estimation and synthesis, Current trends	8Hrs

Text Books

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002.
2. Rabaey, Pedram, “Low power design methodologies” Kluwer Academic, 1997.

Reference Books:

1. A. Chandrakasan and R. Brodersen, “Low Power CMOS Design”.
2. Sung - Mo Kang & Yosuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, TMH, 2003 (Third Edition).
3. Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, “System-on-chip Test Architectures”, 2008.
4. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000.

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Program: VLSI Design & Embedded Systems			Teaching Hours
Course Title: Internet of Things		Course Code: 19EVEE706	
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 25 Hrs	Examination Duration:		

Chapter No. 1 **Introduction to IoT** Defining IoT, Characteristics of IoT, What is the IoT and why is it important? Elements of an IoT ecosystem. Technology and business drivers. IoT applications, trends and implications. Physical design of IoT, Logical design of IoT, Functional blocks of IoT, Communication models & APIs	4
Chapter No. 2 **IoT Architecture: State of the Art** History of IoT, M2M – Machine to Machine, Web of Things, IoT protocols Applications: Remote Monitoring & Sensing, Remote Controlling,Performance Analysis.	4
Chapter No. 3 The Layering concepts , IoT Communication Pattern, IoT protocol Architecture, The 6LoWPAN,Security aspects in IoT	4
Chapter No. 4 **IoT Application Development:** **Application Protocols** MQTT, REST/HTTP, CoAP, MySQL	6
Chapter No.5 **Case Study & advanced IoT Applications:** IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipment's. Use of Big Data and Visualization in IoT, Industry 4.0 concepts.	6
Hands-on Lab **Arduino, Android and AWS based Experiments** 1. AWS Setup and instance creation. 2. Controlling LEDs blinking pattern through UART/WiFi 3. Simple photocell to measure the ambient light level 4. Controlling LEDs blinking pattern through PHP web server. 5. Temperature measurement through ADC and WiFi 6. Controlling and interacting with basic actuators (relay).	

7. Android Application development.
8. Controlling of Arduino embedded system using Android App.
9. Motor Speed control using Embedded board and NodeMCU

Lua Programming Based Experiments

1. Introduction to Lua programming
2. Controlling inbuilt LED of ESP8266
3. Controlling Motion Sensor using NodeMCU module.
4. Using ESP8266 as Webserver
    a. Understanding HTML Tags.
    b. Understanding Request.
    c. Reading Parameter Values.
    d. Controlling LED.
5. ThingSpeak Cloud - Data Visualization
    a. Working with Temperature & Humidity Sensor
    b. Working with ThingSpeak Cloud
    c. Posting & Analyzing Sensor Data on ThingSpeak Cloud

Text Books:

1. Arshdeep Bahga, Vijay Madisetti “Internet of Things (A Hands-on-Approach)” Universities Press- 2014.
2. Olivier Hersent, David Boswarthick, Omar Elloumi, “The Internet of Things: Key Applications and Protocols” John Wiley & Sons – 2012.

Reference Books:

1. Subhas Chandra Mukhopadhyay “Internet of Things Challenges and Opportunities” Springer- 2014.

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Course Code: 20EVEE707	Course Title: AUTOSAR	
L-T-P : 2-0-1	Credits: 3	Contact Hrs: 4 Hours
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 3 hours

Content	Hrs
Chapter No. 1: AUTOSAR Fundamentals Evolution of AUTOSAR – Motivations and Objectives AUTOSAR consortium – Stake holders – work Packages, AUTOSAR Partnership, Goals of the partnership, Organization of the partnership, AUTOSAR specification, AUTOSAR Current development status, BSW Conformance classes: ICC1, ICC2, ICC3, and Drawbacks of AUTOSAR.	8 hrs
Chapter No. 2: AUTOSAR layered Architecture AUTOSAR Basic software, Details on the various layers , Details on the stacks Virtual Function Bus (VFB) Concept Overview of AUTOSAR Methodology , Tools and Technologies for AUTOSAR AUTOSAR Application Software Component (SW-C) ,Types of SW-components AUTOSAR Run Time Environment (RTE): RTE Generation Process: Contract Phase, Generation Phase, MCAL, IO HW Abstraction Layer, Partial Networking, Multicore, J1939 Overview, AUTOSAR Ethernet, AUTOSAR E2E Overview , AUTOSAR XCP, Metamodel , From the model to the process , Software development process.	7 hrs
Chapter No. 3: Methodology of AUTOSAR and Communication in AUTOSAR CAN Communication, CAN FD, CANape, Application Layer and RTE, intra and inter ECU communication, Client-Server Communication, Sender-Receiver, Communication, CAN Driver, Communication Manager (ComM), Overview of Diagnostics Event and Communication Manager	10 hrs
Chapter No. 4: Overview about BSW constituents BSW Constituents: Memory layer, COM and Services layer, ECU abstraction, AUTOSAR, Operating system, Interfaces: Standard interface, AUTOSAR standardized interface, BSW-RTE interface,(AUTOSAR interface), BSW-ECU hardware interface, Complex device drivers and BSW module configuration, AUTOSAR Integration.	5 hrs
Chapter 5: MCAL and ECU abstraction Layer Microcontroller Drivers, Memory drivers: on-chip and off chip drivers, IO drivers(ADC, PWM, DIO), Communication drivers: CAN driver, LIN drivers, Flexrfay	5 hrs
Chapter 6: Service Layer Diagnostic Event Manager, Function inhibits Manager, Diagnostic communication manager, Network management, Protocol data unit router, Diagnostic log and trace unit, COMM manager.	5 hrs
Text Book (List of books as mentioned in the approved syllabus) 1. Ronald K. Jurgen, Infotainment systems, 2007, SAE International, 2007	

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Program: Digital Electronics		
Course Title: Mini Project		Course Code: 19EVEW701
L-T-P-SS: 0-0-3	Credits: 3	Contact Hours: 6
CIE Marks: 50	SEE Marks: 50	Total Marks: 100
	Examination Duration: 3 hours	

1. The project needs to encompass the concepts leant in a courses in the previous semesters, so that the student will learn to integrate, the knowledge acquired to provide a solution to the defined problem statement of the mini-projects.
2. Student can select a project which leads to a product or model or prototype related to following areas (not limited to these areas).
    1. Embedded systems
    2. MEMS
    3. VLSI design
    4. Image processing
    5. Micro controllers
    6. Communications
3. Time plan: Effort to do the project should be between 50 hours,

Semester End Evaluation (SEE)

Semester end examination (SEE) includes submission of the project report, demonstration of the mini-projects and viva-voce conducted by the external and internal examiner. SEE carries 50% weightage of total marks of mini-projects.

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Semester: III Semester M.Tech.

Program: VLSI Design & Embedded Systems		
Course Title: Internship / Mini Project		**Course Code: 17EVEI801**
L-T-P: 0-0-8	**Credits: 8**	**Contact Hours: 16**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
	Examination Duration: 3 hours	

Internship: 6 weeks of training in any reputed industry. A report has to be made and should be submitted at the end of the training.

OR

Mini-Project 3:

1. The project needs to encompass the concepts leant in a courses in the previous semesters, so that the student will learn to integrate, the knowledge acquired to provide a solution to the defined problem statement of the mini-projects.
2. Student can select a project which leads to a product or model or prototype related to following areas (not limited to these areas).
    1. Embedded systems
    2. MEMS
    3. VLSI design
    4. Image processing
    5. Micro controllers
    6. Communications

Semester End Evaluation (ESA)

Semester end examination (ESA) includes submission of the project report, demonstration of the mini-projects and viva-voce conducted by the external and internal examiner. ESA carries 50% weightage of total marks of mini-projects.

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Program: VLSI Design & Embedded Systems		
Course Title: Project Phase I / Minor Project		Course Code: 17EVEW801
L-T-P: 0-0-10	Credits: 10	Contact Hours: 20
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
	Examination Duration: 3 hours	
12 weeks duration shall be carried out. Candidates in consultation with the guides shall carryout literature survey / visit to Industries to finalize the topic of dissertation. Evaluation of the same shall be taken up during end of III Semester.		

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Program: VLSI Design & Embedded Systems		
Course Title: Project Phase II / Major project		Course Code: 17EVEW802
L-T-P: 0-0-20	Credits: 20	Contact Hours: 40
ISA Marks: 50	ESA Marks: 100	Total Marks: 150
	Examination Duration: 3 hours	
24 weeks duration. Evaluation shall be taken during the end of the IV Semester. Need to present three reviews during the project work. Evaluation shall be taken up during the end of IV Semester. At the end of the Semester Project Work Evaluation and Viva-Voce Examinations will be conducted.		

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